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Optimization of Extended Phase-Shift Control for Full-Bridge CLLC Resonant Converter with Improved Light-Load Efficiency

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***Abstract*-The CLLC resonant converters are drawing more and more attention for their superiority in soft switching, wide output range and symmetrically bidirectional operation. However, CLLC converter still suffers the problems of unsatisfactory voltage regulation and low efficiency under light-load conditions. Therefore, this paper proposes an optimization for extended phase-shift (EPS) control in full-bridge CLLC resonant converter to improve the light-load efficiency. In order to study the relations between phase-shifts of EPS control and converter efficiency, a detailed circuit model is first established to solve the voltage gain, time-domain expressions of main circuit variables and root mean square (RMS) values of resonant currents. Then, a comprehensive loss evaluation is conducted by calculating and analyzing the main power losses, including conduction loss, switching loss and core losses of magnetic components. Besides, zero voltage switching (ZVS) conditions of primary and rectifier switches are derived to define the range of soft switching. Finally, based on these analyses, the optimal combination of phase-shifts for EPS control is determined to achieve the maximum conversion efficiency of full-bridge CLLC converter at light-load conditions. The validity of the proposed optimized EPS control is verified on a 18~25V/400V, 200W GaN based CLLC resonant converter prototype.**

***Index Terms*—CLLC resonant converter, extended phase-shift control, light-load efficiency, power loss evaluation, optimization.**

I. Introduction

In recent years, with the rapid development of battery chargers, electric vehicles, uninterrupted power supplies (UPSs), renewable energy sources, energy storage systems, telecom and information systems, aviation power systems, etc., bidirectional DC-DC converters become an important link to interface between a high-voltage DC bus and a low-voltage DC bus, where energy generation devices like a photovoltaic array, and energy storage devices, such as a battery or a super-capacitor, are respectively installed [1-8] , as shown in Fig. 1. For batteries or super-capacitors, their voltages usually vary with the state-of-charge, which requires the bidirectional DC-DC converters to provide a relatively wide output range. Besides, to meet the safety and reliability standards while maintaining the flexibility and maneuverability of power systems, galvanic isolation with a high-frequency transformer is often required [1, 3, 9].

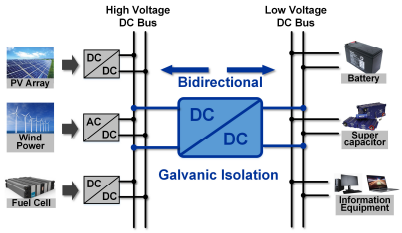

Fig. 1. Typical applications of bidirectional DC-DC converters [1].

Among plenty of isolated bidirectional DC/DC converters, dual active bridge (DAB) is one of the most commonly used topologies because of its bidirectional operation capability, ease of achieving soft-switching and symmetric structure [2]. Nevertheless, the circulating current gets higher when the input and output voltages do not match, leading to a rapid decrease of efficiency [2, 5]. Besides, the soft-switching region becomes limited under light-load conditions [2, 10]. LLC resonant converters can regulate the output voltage under wide load variations with a relatively small range of switching frequency. Zero voltage switching (ZVS) of primary switches and zero current switching (ZCS) of secondary switches could also be achieved for a wide operating range, resulting in high power conversion efficiency [11]. However, conventional LLC converter can only operate in one direction. CLLC (capacitor-inductor-inductor-capacitor) resonant converter, composed of two full-bridges and a symmetrical resonant tank containing two pairs of resonant inductors and resonant capacitors as shown in Fig. 2, has become a promising topology in virtue of its soft switching characteristics, wide output range and bidirectional operation [9]. Moreover, using emerging wide bandgap devices, CLLC resonant converter can increase the switching frequency and achieve higher power density with integrated magnetics [5], [12, 13].

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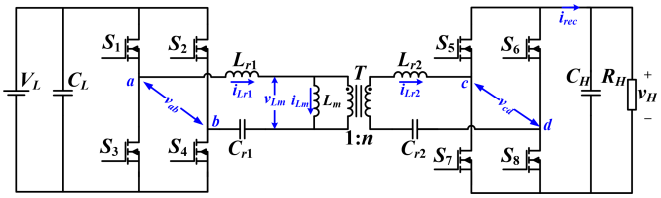


Fig. 2. Topology of full-bridge CLLC resonant converter.

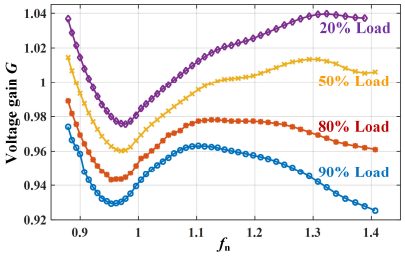


Fig. 3. Voltage gain curve of full-bridge CLLC resonant converter using PFM control (obtained by sweeping frequency experiment on our designed CLLC converter prototype).

With the explosive demands of electric power in the above applications, the efficiency requirement of power conversion is getting higher and higher, which is not only focused on the heavy load but also on the light load [14]. Hence, it's necessary and important to improve the light-load efficiency of bidirectional CLLC resonant converters. CLLC resonant converter faces similar light-load problems of low efficiency and unsatisfying voltage regulation as LLC converters [15-17], especially at high operation frequency. Conventionally, the output voltage of CLLC converter is regulated by modulating the switching frequency, i.e. Pulse Frequency Modulation (PFM) [9]. As presented in Fig. 3, the voltage gain of CLLC converter under light-load conditions rises with the increase of frequency over resonant frequency, while normally the gain should drop with increasing frequency in this region. As a result, the converter could get out of control in the closed loop operation and the switching frequency is adjusted approaching the upper limit, resulting in extremely high switching loss and severely lowering the power conversion efficiency.

To regulate the output voltage and improve the efficiency of resonant converters under light-load conditions, many control methods have been proposed [14-22]. Burst control [14, 18-22] is an effective way to adjust the voltage gain and raise the light-load efficiency by switching the converter between on and off state. The performance of hysteresis burst control for LLC converter greatly depends on the select of hysteresis band [19]. Wide band induces a large output voltage ripple requiring additional filter design, while small band results in a limited burst efficiency. Optimal trajectory control proposed in [14] optimizes the efficiency of burst mode with a three-pulse switching pattern, yet high performance FPGA controller and complex analog circuit are required, making it difficult to be implemented in practice. A simplified optimal trajectory control is presented in [20] to achieve the implementation of adaptive burst control in low cost microcontrollers. However, the switching patterns are still quite complicated. [22] adopts an energy feedback control using synchronous rectifiers (SRs) during the off time of burst control. The SR bridges are controlled ahead of the primary bridges, delivering the energy from load to source and reducing the output voltage, but the phase-shift of SRs should be optimized to balance the voltage regulation capacity and efficiency. [23] regulates the light-load voltage by extending the turn-on time of SRs, which generates a negative current feeding back the power to source. The limitation of this method is that the extension of turn-on time is restricted by half switching cycle, making it non-effective under extreme light-load conditions. In [24], A PWM control strategy for LLC converters is proposed to enlarge the output range through varying the duty ratio of gate signals, while the duty ratio is restrained by ZVS requirements, which further limits the voltage gain. An asymmetric pulse-width modulation is adapted in a half-bridge LLC resonant converter to reduce the core losses of transformer at light-load [25]. Nevertheless, this method aims at voltage doubler rectifier and smaller duty cycle leads to larger turn-off loss and inductor core loss.

Compared with the methods above, phase-shift control is a relatively effective and simple way to improve the light-load efficiency for full-bridge LLC converters [26, 27]. [26] changes the light-load output voltage by regulating the phase-shift between two legs of the primary bridge, yet the losses are not considered and the overall efficiency is not optimized. [27] calculates comprehensively the power losses of phase-shift control and determines the optimal duty ratio adaptive to different load conditions. However, these research are mostly focused on the unidirectional LLC converters. For bidirectional full-bridge CLLC converters, the performance of phase-shift control depends on not only the injection of phase-shift in primary full-bridge, but also the phase-shift of rectifier switches. Hence, the combination of phase-shifts needs optimizing to maximize the overall efficiency.

This paper employs an optimized extended phase-shift (EPS) control for full-bridge CLLC resonant converter to regulate the output voltage and improve the efficiency under light-load conditions. The EPS control introduces an inner phase-shift between primary legs and an outer phase-shift between primary and secondary bridges, as defined in dual active bridge (DAB) [2]. A detailed circuit model is first established to derive the voltage gain, time-domain expressions of main circuit variables and RMS values of resonant currents under EPS control. Then the overall power losses, including the losses of switches and core losses of magnetic components, are computed and analyzed under different inner and outer shifted phases. Through the comprehensive loss analysis, it can be drawn that the CLLC resonant converter has the minimum total power loss when the outer phase-shift is around the half of the inner phase-shift, and achieves the maximum efficiency with the outer phase-shift equal to the half of the inner phase-shift. Moreover, the conclusion about the optimal ratio between the inner and outer phase-shifts is determined by the operating principles and characteristics of EPS control method and is supposed to be valid for full-bridge CLLC resonant converters with different parameters using different power semiconductors. To verify the correctness of

the analysis and conclusion, a 21.5V/400V, 200W GaN based CLLC resonant converter prototype is built and tested.

This paper is organized as follows. Section II describes the operation principles of EPS control in the full-bridge CLLC converter and presents a detailed circuit modeling, calculation and analysis. In Section III, the comprehensive power losses are evaluated, and the optimal phase-shifts of EPS control are determined. Section IV gives the experimental results and conclusions are drawn in Section V.

II. Operation Principles and Detailed Modeling of Full-Bridge CLLC Resonant Converter with EPS Control

In this section, the concept and operation principles of EPS control are first presented. Then the main operational stages are modelled, and the voltage gain, RMS values of two resonant currents are calculated and analyzed based on different combinations of inner and outer phase-shifts.

A. Operation principles of EPS control in full-bridge CLLC converter

The circuit configuration of full-bridge CLLC resonant converter is shown in Fig. 2, and the key waveforms are illustrated in Fig. 4. V_L is the low voltage input, V_H is the high voltage output and v_H is the instantaneous output voltage. v_{ab} and v_{cd} are the mid point voltages of primary and secondary full-bridges, and v_{Lm} is the voltage of magnetizing inductance. i_{r1} and i_{r2} are respectively resonant currents of resonant inductor L_{r1} and L_{r2}. i_{Lm} is the magnetizing current of the transformer and i_{rec} is the output current of rectifier full-bridge. n is the turns ratio of the transformer. In EPS control, the inner phase-shift D_1T_r is added for the primary leg of S_2 and S_4, making this phase leg lagging behind S_1 and S_3. The rectifier bridge $S_{5\text{-}8}$ are also controlled behind S_1 and S_3 with an outer phase-shift D_2T_r. Since the operational principles of two half cycles are symmetrical, only a half cycle is explained in detail. According to the switching patterns of S_1-S_8, each half switching period can be divided into three operation modes, and the circuit diagram of each mode is presented in Fig. 5. The time durations of three modes are defined as follows:

$$T_1 = t_1 - t_0 = \left(\frac{1}{2} - D_1\right)T_r, T_2 = t_2 - t_1 = D_2T_r, T_3 = t_3 - t_2 = (D_1 - D_2)T_r \quad (1)$$

where T_r is the resonant period, D_1 is the ratio of inner phase-shift, D_2 is the ratio of outer phase-shift, T_1, T_2, T_3 are time durations of three operation modes.

Mode I ($t_0 - t_1$): Before t_0, S_1 and S_2 are on and $v_{ab} = 0$. At t_0, S_2 is turned off. The negative i_{r1} makes S_4 conduct reversely and discharges the output capacitance of S_4, creating the ZVS condition for its switching on. Then, v_{ab} increases to V_L. After the dead-time, S_4 is turned on and i_{r1} rises across zero. v_{ab} remains at V_L. L_{r1} and C_{r1} resonate, transferring the input power to the output, and the resonant current i_{r1} is close to a sine. Hence i_{r1} can be approximately written in a sinusoidal form as (2). Because S_5 and S_8 are on-state during this period, v_{cd} equals V_H. The voltage of magnetizing inductance v_{Lm} can be approximated as V_L since the voltage drop across L_{r1} and

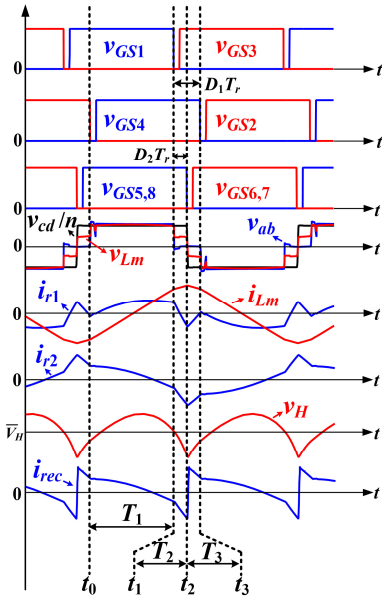
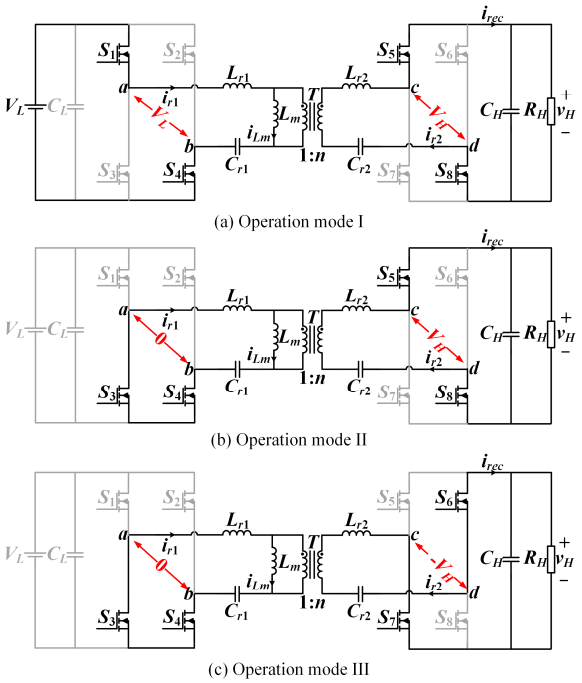


Fig. 4. Key waveforms of CLLC resonant converter using EPS control.



(a) Operation mode I

(b) Operation mode II

(c) Operation mode III

Fig. 5. Circuit diagram of different operation modes.

C_{r1} is close to 0 due to their resonance. The magnetic current i_{Lm} can be considered linearly increasing with a slope of V_L/L_m as (3) [27]. The voltage of L_{r1} can be obtained by (4).

$$i_{r1}(t) = i_{r1}(t_0)\cos\omega_r(t - t_0) + \frac{V_L - \frac{V_H}{n} - v_{C_{r1}}(t_0)}{Z_r}\sin\omega_r(t - t_0) \quad (2)$$

$$i_{L_m}(t) = i_{L_m}(t_0) + \frac{v_{L_m}(t_0)}{L_m}(t - t_0) \approx i_{L_m}(t_0) + \frac{V_L}{L_m}(t - t_0) \quad (3)$$

$$v_{L_{r1}}(t)=\left[V_L-\frac{V_H}{n}-v_{C_{r1}}(t_0)\right]\cos\omega_r(t-t_0)-Z_r\,i_{r1}(t_0)\sin\omega_r(t-t_0) \tag{4}$$

where ω_r is the resonant frequency, $Z_r=\sqrt{L_{r1}/C_{r1}}$ is the resonant impedance, L_m is the magnetizing inductance.

Mode II (t_1 – t_2): At t_1, S_1 is turned off. S_3 is softly switched on after the output capacitance discharge during the dead-time, forced by the positive i_{r1}. Then v_{ab} falls to 0, while v_{cd} is still V_H. Since the resonant tank is symmetric, the resonant impedances of L_{r1}, C_{r1} and L_{r2}, C_{r2} are the same with the secondary side of transformer equivalent to the primary side. Hence, the voltage drops across L_{r1}, C_{r1} and across L_{r2}, C_{r2} are both equal to $-V_H/(2n)$, and the voltage v_{Lm} across the magnetizing inductance changes to $V_H/(2n)$. During this period, L_{r1} and C_{r1} no longer resonate. The negative voltage on L_{r1} induces the resonant current i_{r1} to decrease approximately linearly as (5), and i_{Lm} keeps increasing with the slope of $V_H/(2nL_m)$ as (6).

$$i_{r1}(t)=i_{r1}(t_1)-\frac{\frac{V_H}{2n}+v_{C_{r1}}(t_1)}{L_{r1}}(t-t_1) \tag{5}$$

$$i_{L_m}(t)=i_{L_m}(t_1)+\frac{V_H}{2nL_m}(t-t_1) \tag{6}$$

Mode III (t_2 – t_3): At t_2, S_5 and S_8 are turned off and v_{cd} drops to $-V_H$ due to the reverse conduction of S_6 and S_7 in the dead-time. Because S_3 and S_2 are kept at on state, v_{ab} remains zero. Similar to mode II, the voltage drops across L_{r1}, C_{r1} and across L_{r2}, C_{r2} are both equal to $V_H/(2n)$, and v_{Lm} decreases to $-V_H/(2n)$. Therefore, i_{r1} rises as (7) under the positive voltage and i_{Lm} falls linearly with the slope of $-V_H/(2nL_m)$ as (8).

$$i_{r1}(t)=i_{r1}(t_2)+\frac{V_H/(2n)-v_{C_{r1}}(t_3)}{L_{r1}}(t-t_2) \tag{7}$$

$$i_{L_m}(t)=i_{L_m}(t_2)-\frac{V_H}{2nL_m}(t-t_2) \tag{8}$$

B. Calculation of voltage gain and RMS values of resonant currents

The voltage gain and RMS values of two resonant currents of full-bridge CLLC converter using EPS control can be derived based on the modeling in part *A*.

The averaging output current I_o can be calculated as follows:

$$\begin{aligned}I_o&=\frac{V_H}{R_H}=\frac{2}{T_r}\left[\int_{t_0}^{t_2}i_{r2}(t)dt-\int_{t_2}^{t_3}i_{r2}(t)dt\right]\\&=\frac{2}{nT_r}\left[\left(\int_{t_0}^{t_2}i_{r1}dt-\int_{t_2}^{t_3}i_{r1}dt\right)-\left(\int_{t_0}^{t_2}i_{L_m}dt-\int_{t_2}^{t_3}i_{L_m}dt\right)\right]\\&=\frac{I_{in}}{n}-\frac{T_1(T_2-T_3)}{nT_rL_m}\left(V_L-\frac{V_H}{2n}\right)\end{aligned} \tag{9}$$

where I_{in} is the average value of input current.

Since the operation principle is symmetric per half period, the capacitor voltage v_{Cr1} has opposite values at t_0 and $t_0+T_r/2$, which is expressed as (10).

$$\begin{aligned}-v_{C_{r1}}(t_0)&=v_{C_{r1}}(t_0+T_r/2)\\&=v_{C_{r1}}(t_0)+\frac{1}{C_{r1}}\int_{t_0}^{t_0+\frac{T_r}{2}}i_{r1}(t)dt\\&=v_{C_{r1}}(t_0)+\frac{1}{C_{r1}}\left[\frac{T_r}{2}I_{in}+\int_{t_1}^{t_3}i_{r1}(t)dt\right]\\&=\frac{T_rI_{in}}{2C_{r1}}-v_{C_{r1}}(t_1)\end{aligned} \tag{10}$$

From (9) and (10), $v_{Cr1}(t_1)$ can be obtained by cancelling the variable I_{in} as (11).

$$v_{C_{r1}}(t_1)=\frac{T_r}{2C_{r1}}\left[\frac{n}{R_H}-\frac{(T_2-T_3)T_1}{2nL_mT_r}\right]V_H+\frac{(T_2-T_3)T_1}{2L_mC_{r1}}V_L+v_{C_{r1}}(t_0) \tag{11}$$

By using the voltage expression of L_{r1} in (4), v_{Cr1} at t_1 can also be derived as:

$$\begin{aligned}v_{C_{r1}}(t_1)&=-v_{L_{r1}}(t_1)\\&=\left(\frac{V_H}{n}-V_L\right)\cos\omega_rT_1+v_{C_{r1}}(t_0)\cos\omega_rT_1+i_{r1}(t_0)Z_r\sin\omega_rT_1\end{aligned} \tag{12}$$

Similarly, the waveform of resonant current i_{r1} is negatively symmetrical over two half cycles as well. Hence, $i_{r1}(t_0)$ equals $-i_{r1}(t_3)$, as shown in (13), where $i_{r1}(t_3)$ can be substituted based on (7) and $i_{r1}(t_2)$ can be replaced by (5).

$$\begin{aligned}i_{r1}(t_0)&=-i_{r1}(t_3)\\&=-i_{r1}(t_2)-\frac{\frac{V_H}{2n}-v_{C_{r1}}(t_3)}{L_{r1}}T_3\\&=-i_{r1}(t_1)+\frac{\frac{V_H}{2n}+v_{C_{r1}}(t_1)}{L_{r1}}T_2-\frac{\frac{V_H}{2n}-v_{C_{r1}}(t_3)}{L_{r1}}T_3\end{aligned} \tag{13}$$

By further substituting $i_{r1}(t_1)$ according to (2), equation (13) is finally simplified as (14).

$$\begin{aligned}&\left(\frac{\sin\omega_rT_1}{nZ_r}+\frac{T_2}{2nL_{r1}}-\frac{T_3}{2nL_{r1}}\right)V_H-(1+\cos\omega_rT_1)i_{r1}(t_0)+\\&\left(\frac{\sin\omega_rT_1}{Z_r}-\frac{T_3}{L_2}\right)v_{C_{r1}}(t_0)+\frac{T_2}{L_2}v_{C_{r1}}(t_1)-\frac{\sin\omega_rT_1}{Z_r}V_L=0\end{aligned} \tag{14}$$

To facilitate the calculation, a practical approximate condition is proposed: the time instant t_x of zero crossing of i_{r2} is approximately a quarter of switching cycle from the rising edge of $v_{GS5,8}$ at light-load conditions, as given in (15).

$$t_x\approx T_d-T_3+\frac{T_r}{4},\quad i_{r1}(t_x)=i_{L_m}(t_x) \tag{15}$$

where T_d is the period of dead-time.

By utilizing the expressions (2)-(3) of i_{r1} and i_{Lm} of mode I, (15) can be written as:

$$i_{r1}(t_0)\cos\omega_rt_x+\frac{V_L-\frac{V_H}{n}-v_{C_{r1}}(t_0)}{Z_r}\sin\omega_rt_x=-I_{m0}+\frac{V_L}{L_m}t_x \tag{16}$$

where I_{m0} is the absolute value of magnetizing current i_{Lm} at t_0 and can be derived according to (3), (6), (8) as follows:

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$$I_{m0} = -I_{m0} + \frac{V_L}{L_m}T_1 + \frac{T_2 - T_3}{2nL_m}V_H \tag{17}$$

Combining and reorganizing (11)-(12), (14) and (16), a four-dimensional matrix equation can be extracted:

$$Ax = A\begin{bmatrix} i_{r1}(t_0) \\ v_{C_{r1}}(t_0) \\ v_{C_{r1}}(t_1) \\ V_H \end{bmatrix} = b = \begin{bmatrix} \dfrac{(T_3 - T_2)T_1}{2L_m C_{r1}}V_L \\ \dfrac{\sin\omega_r T_1}{Z_r}V_L \\ V_L\cos\omega_r T_1 \\ V_L\left(\dfrac{2t_x - T_1}{2L_m} - \dfrac{\sin\omega_r t_x}{Z_r}\right) \end{bmatrix} \tag{18}$$

where,

$$A = \begin{bmatrix} 0 & 1 & -1 & \dfrac{T_r}{2C_{r1}}\left[\dfrac{n}{R_H} - \dfrac{(T_2 - T_3)T_1}{2nL_m T_r}\right] \\ -(1+\cos\omega_r T_1) & \left(\dfrac{\sin\omega_r T_1}{Z_r} - \dfrac{T_3}{L_2}\right) & \dfrac{T_2}{L_2} & \left(\dfrac{\sin\omega_r T_1}{nZ_r} + \dfrac{T_2 - T_3}{2nL_{r1}}\right) \\ Z_r\sin\omega_r T_1 & \cos\omega_r T_1 & -1 & \dfrac{\cos\omega_r T_1}{n} \\ \cos(\omega_r t_x) & -\dfrac{\sin(\omega_r t_x)}{Z_r} & 0 & \left(\dfrac{T_2 - T_3}{4nL_m} - \dfrac{\sin\omega_r t_x}{nZ_r}\right) \end{bmatrix} \tag{19}$$

Consequently, by calculating the inverse matrix of A, the solution of the above matrix equation is $x=A^{-1}b$. With x solved, the values of four variables $i_{r1}(t_0)$, $v_{Cr1}(t_0)$, $v_{Cr1}(t_1)$, V_H are known, and the time-domain piecewise numerical expressions of two resonant currents can be obtained according to equations (2)-(8).

As a result, the voltage gain G is calculated as:

$$G = \frac{V_H}{nV_L} \tag{20}$$

And the RMS values of two resonant currents, I_{r1_RMS} and I_{r2_RMS} are respectively calculated using time-domain expressions (2)-(8) of i_{r1} and i_{Lm}.

$$\begin{aligned} I_{r1\_RMS} &= \frac{2}{T_r}\sqrt{\int_{t_0}^{t_0+T_r/2} i_{r1}^2(t)dt} \\ I_{r2\_RMS} &= \frac{2}{T_r}\sqrt{\int_{t_0}^{t_0+T_r/2}\left[\left(i_{r1}(t) - i_{L_m}(t)\right)/n\right]^2 dt} \end{aligned} \tag{21}$$

To study the influences of D_1, D_2 on the voltage gain and RMS of resonant currents, different values of D_1 and D_2 are substituted into the matrix equation (18)-(19) to solve G, I_{r1_RMS} and I_{r2_RMS}. Fig. 6 shows the time-domain waveforms of i_{r1} and i_{r2} in a half switching cycle with D_1=0.12, D_2=0.03~0.09 at 20% load. It can be observed that when D_2 deviates from $0.5D_1$, the magnitudes of i_{r1} increases. For i_{r2}, its smallest magnitude is distributed at D_2 close to $0.5D_1$.

The relationships between I_{r1_RMS}, I_{r2_RMS} and D_1, D_2 under 20% load are respectively demonstrated in Fig. 7 and Fig. 8. For a certain value of D_1 between 0~0.2, I_{r1_RMS} always gets minimum at D_2=$0.5D_1$ and increases with the deviation of D_2 from $0.5D_1$, while the minimum value of I_{r2_RMS} appears at D_2<$0.5D_1$. Since I_{r1_RMS} is much larger than I_{r2_RMS}, the conduction loss of primary switches dominates the whole conduction loss which also gets its lowest value around D_2=$0.5D_1$.

The voltage gain of CLLC converter using EPS control at 20% load is depicted in Fig. 9. The gain decreases with the rise of D_1. For a certain D_1, when D_2 increases, the voltage gain first augments and then falls.

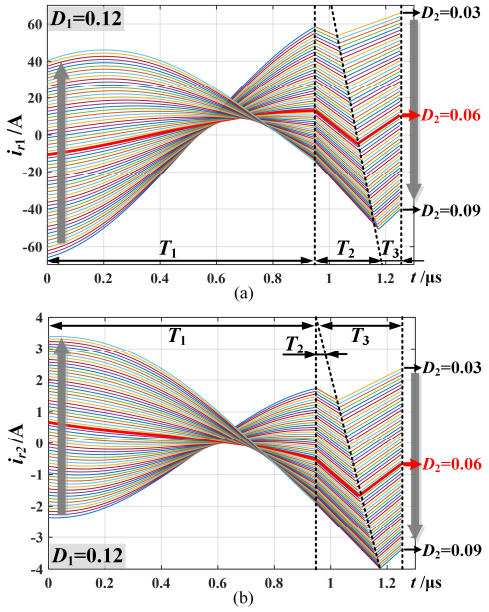

Fig. 6. Half cycle waveforms of resonant currents with D_1=0.12, D_2=0.03~0.09 at 20% load. (a) i_{r1}. (b) i_{r2}.

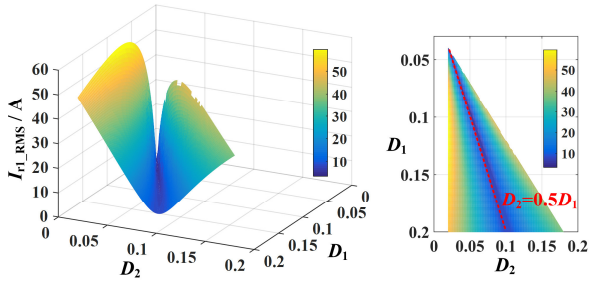

Fig. 7. Relationship between I_{r1_RMS} and D_1, D_2 under 20% load. (a) D_1-D_2-I_{r1_RMS} view. (b) D_1-D_2 view.

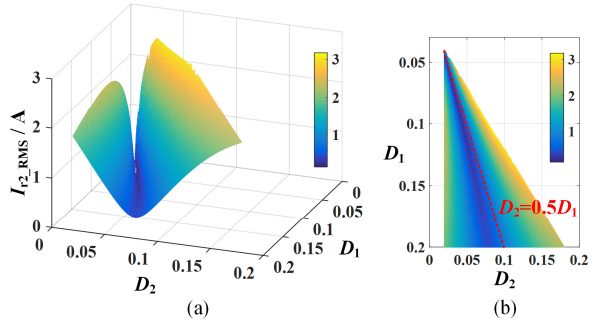

Fig. 8. Relationship between I_{r2_RMS} and D_1, D_2 under 20% load. (a) D_1-D_2-I_{r2_RMS} view. (b) D_1-D_2 view.

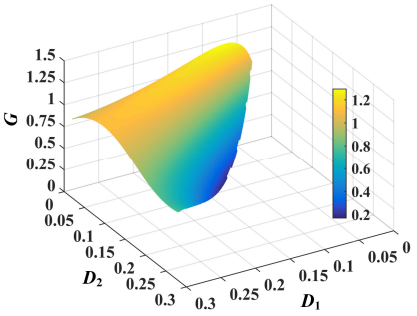

Fig. 9. Voltage gain of CLLC converter using EPS control under 20% load.

III. Loss Analysis for Phase-Shift Optimization of EPS Control

For EPS control in full-bridge CLLC converter, the inner phase-shift D_1T_r is modulated by the closed loop control to achieve the objective voltage, while the outer phase-shift D_2T_r greatly influences the ZVS performance and efficiency of CLLC converter. In order to select the optimal outer ratio D_2 to get the maximum efficiency, the main power losses are evaluated and analyzed based on different values of D_2. Besides, the range of ZVS is also discussed. The parameters of the experimental prototype are used in the following analysis, as listed in Table I.

TABLE I
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter		value	Parameter		Value
V_L		21.5V	f_r		400kHz
L_{r1}		0.0877μH	L_{r2}		31.7μH
C_{r1}		1.8μF	C_{r2}		5nF
T	Core	E32/6/20	n		19
	$N_P : N_S$	1 : 19		Core	EQ20/6.3/14
	L_m	0.4385μH		N_2	13.5
	A_e	130mm^2		A_{e2}	59mm^2
	V_e	4560mm^3		V_{e2}	1960mm^3
	Primary winding	Foil conductor, 0.2mm, 1 turn	L_{r2}	L_{ext2}	25.73μH
				Winding	Litz wire, 0.15mm*17, 13.5 turns
		R_{ac1}=0.868mΩ			R_{ac_Lr2}=37.5mΩ
	Secondary winding	Litz wire, 0.15mm*17, 19 turns	L_{r1}	*winding*	Litz wire, 0.1mm*100, 1 turn
		R_{ac2}=0.1686Ω			R_{ac_Lr1}=2.9mΩ

A. Conduction loss

The conduction loss of the primary and rectifier switches is given in (22).

$$P_{cond} = 2I_{r1\_RMS}^2 R_{dson\_L} + 2I_{r2\_RMS}^2 R_{dson\_H} \tag{22}$$

where R_{dson_L} and R_{dson_H} are respectively the on-resistances of low voltage and high voltage side switches. Since the low voltage side switch is consisted of two parallel GaN devices, R_{dson_L} represents the total on-resistance. I_{r1_RMS} and I_{r2_RMS} are calculated using (21) based on the circuit modeling in section II. The conduction losses of transformer and resonant inductors is negligible, because according to Dowell's model [28-30], the calculated ac resistances of windings are relatively small, as shown in Table. I.

B. Turn-off switching loss

Assuming that ZVS is achieved for primary and rectifier switches, only turn-off loss is considered. As shown in Fig. 4, S_1 is turned off at t_1, S_4 is turned off at t_3 and $S_{5,8}$ are switched off at t_2. Considering the energy exchange of output capacitor during the turn-off process [27, 31] as illustrated in Fig. 10, the turn-off current i_{off1} of S_1 at t_1 is equal to the difference between the resonant current i_{r1} at t_1 and the discharging current i_{dis3} of drain-source capacitance C_{OSSL} of S_3 [27, 31].

$$i_{off1}(t_1) = i_{r1}(t_1) - i_{dis3} = i_{r1}(t_1) - C_{OSSL} V_L / t_{f\_L} \tag{23}$$

where C_{OSSL}=140pF is the output capacitance of low voltage side switch and the turn-off time t_{f_L} can be calculated as [27]:

$$t_{f\_L} = \frac{R_{g\_L} Q_{gd\_L}}{V_{gs,miller\_L}} \tag{24}$$

where R_{g_L} is the gate resistance of S_1, Q_{gd_L} is the gate-drain charge of S_1 and $V_{gs,miller\_L}$ is Miller plateau voltage of S_1.

Assuming that the turn-off current i_{off1} of S_1 is linearly decreased and the drain-source voltage v_{ds1} of S_1 is also linearly increased, the turn-off loss of S_1 can be derived through an integral during the turn-off time:

$$P_{off1} = \frac{1}{T_r}\int_{t_1}^{t_1+t_{f\_L}} i_{off1}(t) v_{ds1}(t) dt = \frac{1}{T_r}\int_0^{t_{f\_L}} \left[i_{off1}(t_1) - k_1 t\right] \cdot k_2 t dt \tag{25}$$

where k_1 and k_2 are respectively the slopes of $i_{off1}(t)$ and $v_{ds1}(t)$:

$$k_1 = i_{off1}(t_1) / t_{f\_L}, \quad k_2 = V_L / t_{f\_L} \tag{26}$$

Hence, the turn-off loss of S_1 is finally written as below [27, 31]:

$$P_{off1} = \frac{1}{6}\left[i_{r1}(t_1) - C_{OSSL} V_L / t_{f\_L}\right] V_L t_{f\_L} f_r \tag{27}$$

The turn-off losses of the rest switches can be calculated similarly as P_{off1} of S_1. Since the low voltage side switch is consisted of two parallel GaN devices, the turn-off losses of low voltage full-bridge P_{off_L} and high voltage full-bridge P_{off_H} can be respectively expressed as:

$$\begin{aligned} P_{off\_L} &= \frac{2}{3}\left|i_{r1}(t_1)\right| - C_{OSSL} V_L / t_{f\_L} \left| V_L t_{f\_L} f_r + \frac{2}{3}\right|i_{r1}(t_0)\left| - C_{OSSL} V_L / t_{f\_L} \right| V_L t_{f\_L} f_r \\ P_{off\_H} &= \frac{2}{3}\left|i_{r2}(t_2)\right| - C_{OSSH} V_H / t_{f\_H} \left| V_H t_{f\_H} f_r \right. \end{aligned} \tag{28}$$

where C_{OSSH}=17pF is the output capacitance of high voltage side switch and t_{f_H} is the turn-off time of high voltage side

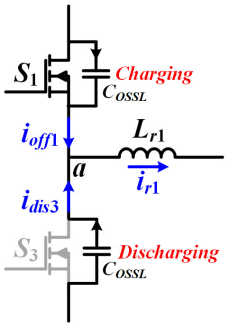

Fig. 10. Turn-off process of switch S_1.

switch. $i_{r1}(t_0)$, $i_{r1}(t_1)$ and $i_{r2}(t_2)$ can be obtained through the time-domain numerical expressions (2)-(8) of resonant currents.

Then the total turn-off loss is:

$$P_{off} = P_{off\_H} + P_{off\_L} \tag{29}$$

C. Core loss of the transformer

The calculation of the transformer core loss is based on the improved generalized Steinmetz equation (IGSE) [32]. Since the waveforms of v_{Lm} in two half cycles are symmetric, the core loss of transformer can be calculated as follows [27]:

$$P_{core\_T} = \frac{2V_e}{T_r}\int_{t_0}^{t_0+T_r/2} k_i \left|\frac{dB_T(t)}{dt}\right|^{\alpha} \left(\Delta B_T\right)^{\beta-\alpha} dt \tag{30}$$

The coefficient k_i is calculated as:

$$k_i = \frac{K}{(2\pi)^{\alpha-1}\int_0^{2\pi}\left|\cos\theta\right|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{31}$$

where V_e is the volume of the transformer core, K, α, β are coefficients determined by characteristics of the magnetic material, ΔB_T is the peak-to-peak magnetic induction and dB_T/dt is the changing rate of magnetic induction.

Based on v_{Lm}, the peak-to-peak magnetic induction ΔB_T is derived as:

$$\Delta B_T = \frac{V_L T_1 + \frac{V_H}{2n}T_2 + \frac{V_H}{2n}T_3}{N_P A_e} \tag{32}$$

where N_P represents the turns of primary windings and A_e is the effective cross-sectional area of the transformer.

The changing rate of magnetic induction dB_T/dt is given as:

$$\frac{dB_T(t)}{dt} = \begin{cases} \dfrac{V_L}{N_P A_e}, & t\in[t_0,t_1] \\ \dfrac{V_H}{2nN_P A_e}, & t\in[t_1,t_2] \\ -\dfrac{V_H}{2nN_P A_e}, & t\in[t_2,t_3] \end{cases} \tag{33}$$

D. Core loss of the external resonant inductor

Since the value of L_{r1} is quite small, L_{r1} is realized by one turn of litz wire without using a magnetic core. The core loss of the external resonant inductor L_{ext2} can be similarly calculated as the transformer core loss in (31).

$$P_{core\_L_{ext2}} = \frac{2V_{e2}}{T_r}\int_{t_0}^{t_0+T_r/2} k_i \left|\frac{dB_{L_{ext2}}(t)}{dt}\right|^{\alpha} \left(\Delta B_{L_{ext2}}\right)^{\beta-\alpha} dt \tag{34}$$

where the peak-to-peak magnetic induction ΔB_{Lext2} and the changing rate of magnetic induction dB_{Lext2}/dt are supposed to be derived based on the external inductance L_{ext2}, instead of the whole resonant inductance L_{r2} [27, 32] as follows:

$$\begin{aligned} \Delta B_{L_{ext2}} &= \frac{2L_{ext2}I_{r2\_\max}}{N_2 A_{e2}} \\ \frac{dB_{L_{ext2}}(t)}{dt} &= \frac{L_{ext2}}{L_{r2}}\frac{v_{L_2}(t)}{N_2 A_{e2}} = \frac{L_{ext2}}{N_2 A_{e2}}\frac{di_{r2}(t)}{dt} \end{aligned} \tag{35}$$

With the results above, the total power loss is written as:

$$P_{loss} = P_{cond} + P_{off} + P_{core\_T} + P_{core\_L_{ext2}} \tag{36}$$

And the overall efficiency of CLLC converter using EPS control can be derived as:

$$\eta = \frac{V_H^2}{R_H}\Big/\left(\frac{V_H^2}{R_H} + P_{loss}\right) \tag{37}$$

From the expression of η, it can be noted that the efficiency is not only determined by the value of power loss, but also influenced by the voltage gain.

To give an intuitive illustration of the relation between efficiency η and outer ratio D_2, Fig. 11 and Fig. 12 describe the power loss distribution and the efficiency curve under 10% and 20% load with D_1=0.12 and D_2=0.04~0.08. It can be observed that the inductor core loss and turn-off switching loss are relatively small compared with the core loss of transformer and the conduction loss. The core loss of transformer varies little with different D_2, while the conduction loss first gets reduced and then augments, varying in consistence with the change of I_{r1_RMS} as aforementioned. Hence, the changing

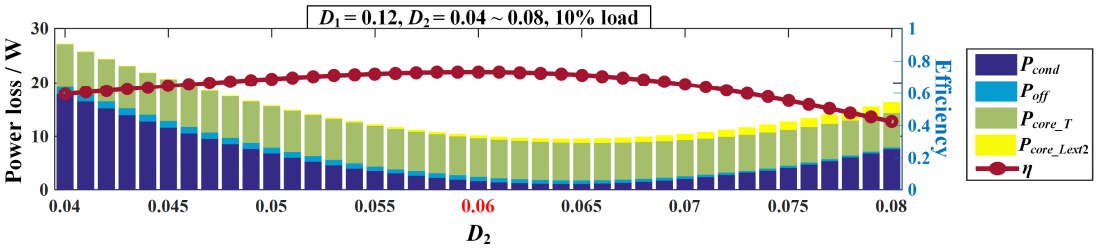

Fig. 11. Power loss distribution and efficiency curve (D_1 = 0.12, D_2 = 0.04~0.08, 10% load).

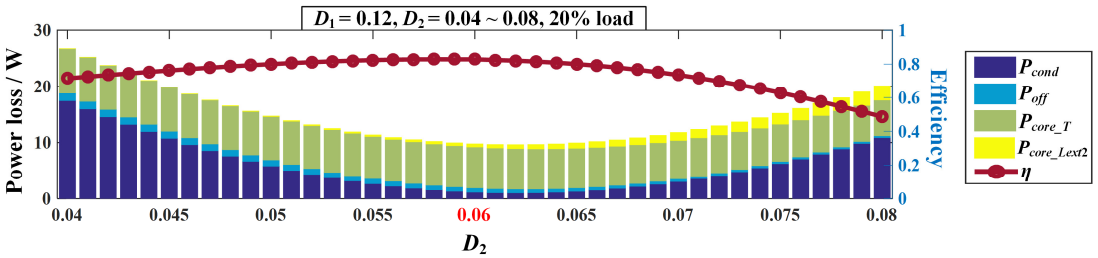

Fig. 12. Power loss distribution and efficiency curve (D_1 = 0.12, D_2 = 0.04~0.08, 20% load).

trend of the overall power loss with D_2 is mainly determined by the variation of conduction loss, which means that the CLLC converter using EPS control has the minimum total power loss around D_2=0.5D_1 and the maximum efficiency is achieved at D_2=0.5D_1.

E. ZVS conditions

To achieve the ZVS of all switches, the sign requirements of resonant currents should first be satisfied. i_{r1} should be negative during the dead-time t_0~t_0+T_d (i.e. positive during t_3~t_3+T_d) to discharge the output capacitances of S_1 and S_4, and is supposed to be positive between t_1~t_1+T_d to ensure the ZVS of S_2 and S_3. To achieve the soft switching of rectifier switches $S_{5\text{-}8}$, i_{r2} should be negative during the dead-time t_2~t_2+T_d. Moreover, the resonant currents must be large enough to fully discharge the output capacitances of the switches before they are turned on. Since the resonant currents are approximately linear and monotonic during the dead-time periods, the ZVS region can be restricted by judging the sign and value of resonant currents at the start and end instants of the dead-times. Hence, these ZVS conditions can be summarized as below:

$$\begin{cases} i_{r1}(t_0)<0 \ \ \& \ \ i_{r1}(t_0+T_d)<0 \\ i_{r1}(t_1)>0 \ \ \& \ \ i_{r1}(t_1+T_d)>0 \\ i_{r2}(t_2)<0 \ \ \& \ \ i_{r2}(t_2+T_d)<0 \\ |i_{r1}(t_0)|>2C_{OSSL}V_L/T_d \ \& \ |i_{r1}(t_0+T_d)|>2C_{OSSL}V_L/T_d \\ |i_{r1}(t_1)|>2C_{OSSL}V_L/T_d \ \& \ |i_{r1}(t_1+T_d)|>2C_{OSSL}V_L/T_d \\ |i_{r2}(t_2)|>C_{OSSH}V_H/T_d \ \& \ |i_{r2}(t_2+T_d)|>C_{OSSH}V_H/T_d \end{cases} \tag{38}$$

where C_{OSSL} and C_{OSSH} are respectively the output capacitances of primary and rectifier switches, T_d is the period of dead-time.

Fig. 13 shows the ZVS region under 10% load with different D_1 and D_2, according to the calculated result of (39). For a certain value of D_1, the range of ZVS is always distributed around D_2=0.5D_1.

As a result, it can be concluded that the optimized phase-shift combination for EPS control in CLLC converter is keeping D_2=0.5D_1, where the CLLC converter gets the maximum efficiency with ZVS achieved. This conclusion of the optimal ratio between D_2 and D_1 is determined by the operating principles and characteristics of EPS control method and is supposed to be valid for full-bridge CLLC resonant converters with different parameters using different power semiconductors.

IV. Experimental Verifications

To confirm the correctness of the above analysis and conclusion, a 18~25V/400V, 200W full-bridge CLLC converter prototype is designed and built as shown in Fig. 14, with the main parameters listed in Table I. GaN devices GS66502B and GS61004B are respectively utilized as the high voltage side switches and the low voltage side switches to increase the resonant frequency and achieve higher power density with reduced and integrated magnetics.

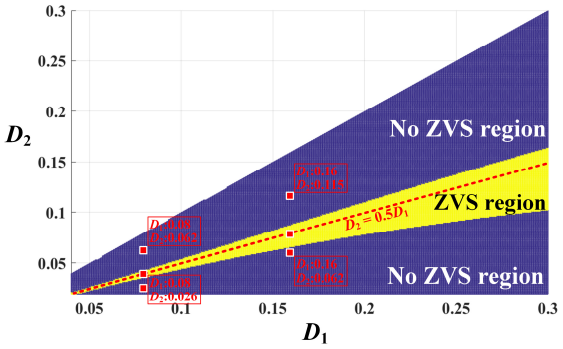

Fig. 13. ZVS region under 10% load.

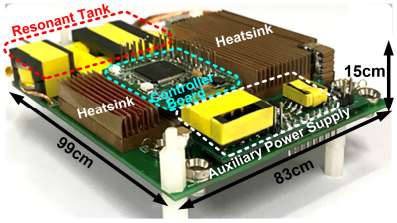

Fig. 14. Experimental prototype.

A. Open-loop experiments

First, open-loop experiments are conducted with different values of D_1 and D_2 to observe their influences on ZVS characteristics, voltage gain, resonant currents and efficiency of CLLC converter.

The ZVS conditions are firstly verified by experiments. Fig. 15 shows the EPS waveforms under 10% load with D_1=0.08 and D_2=0.026, 0.04, 0.062. It can be seen that ZVS of primary switches is achieved at D_2=0.04, yet lost at D_2=0.026 and 0.062. This result is in accord with the derived distribution of ZVS region shown in Fig. 13, where D_2=0.026 and 0.062 are located in the No ZVS Region and D_2=0.04 is distributed in the ZVS Region. Fig. 16 presents the waveforms of EPS control under 10% load with D_1=0.16 and D_2=0.062, 0.08, 0.115. Similarly, the primary switches are softly switched at D_2=0.08, and hard switched at D_2=0.062 and 0.115, which is also consistent with the calculated ZVS distribution in Fig. 13, proving the validity of the ZVS conditions.

Then, the calculated resonant currents based on circuit modeling are verified by experimental waveforms. Fig. 16 shows the comparison of experimental and analytical current waveforms of EPS control under 10% load with D_1=0.16 and D_2=0.062, 0.08, 0.115. It is illustrated that the calculated resonant currents are highly consistent with the experimental waveforms under different D_2, demonstrating the correctness of the analytical time-domain expressions of resonant currents. Both in Fig. 15 and Fig. 16, the magnitudes of resonant current i_{r1} at D_2≠0.5D_1 are much larger than the magnitude of i_{r1} at D_2=0.5D_1. Fig. 17 (b, c) shows the experimental results of RMS values of resonant currents I_{r1_RMS} and I_{r2_RMS}, as well as turn-off currents using EPS control in CLLC converter, with D_1 = 0.08 and D_2 = 0.01~0.08 at 10% load. I_{r1_RMS} has the minimum value at D_2=0.5D_1, and I_{r2_RMS} gets larger when D_2

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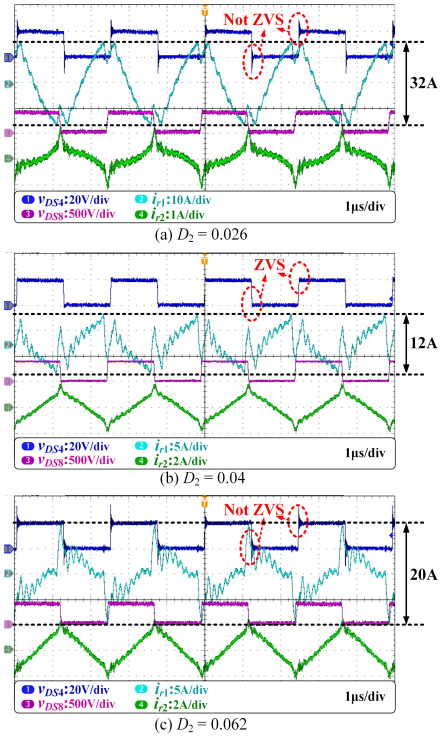
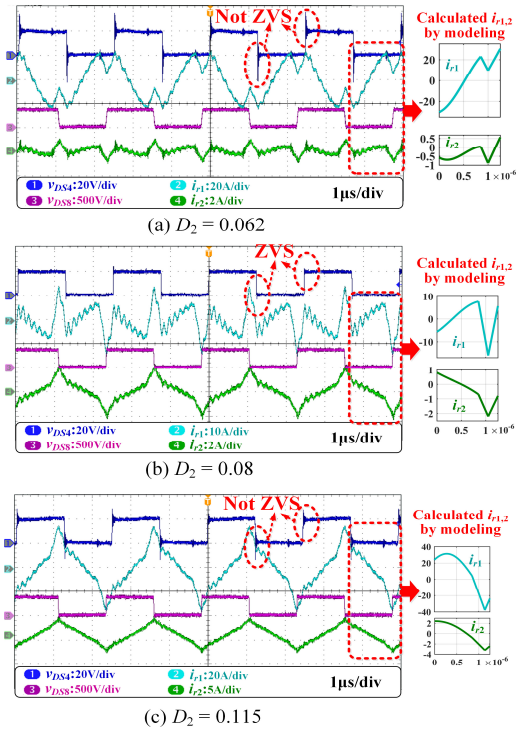


(a) D_2 = 0.026
(b) D_2 = 0.04
(c) D_2 = 0.062

Fig. 15. EPS waveforms under 10% load with D_1=0.08 and different D_2. (a) D_2=0.026. (b) D_2=0.04. (c) D_2=0.062.



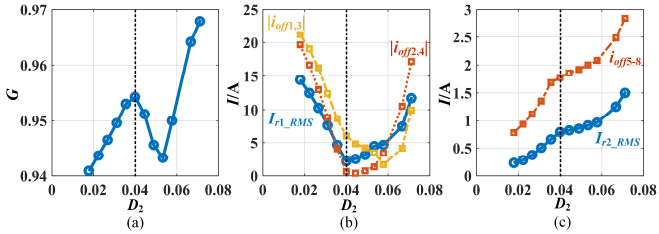
(a) D_2 = 0.062
(b) D_2 = 0.08
(c) D_2 = 0.115

Fig. 16. Experimental and analytical EPS waveforms under 10% load with D_1=0.16 and different D_2. (a) D_2=0.062. (b) D_2=0.08. (c) D_2=0.115.

increases. Fig. 18 (b, c) gives the similar experimental results with D_1 = 0.08 and D_2 = 0.01~0.08 at 30% load. Since the load gets heavier, I_{r1_RMS} and I_{r2_RMS} are both slightly larger than their values at 10% load. Fig. 19 (b, c) presents the experimental results of currents with D_1 = 0.16 and D_2 = 0.06~0.12 at 10% load. Larger D_1 leads to higher values of I_{r1_RMS} and I_{r2_RMS}. According to these results, it can be drawn that under different D_1 and load conditions, I_{r1_RMS} always gets the minimum at D_2=0.5D_1, and I_{r2_RMS} gets larger with the increase of D_2, which also verifies the calculated variation of I_{r1_RMS} and I_{r2_RMS} in Fig. 7 and Fig. 8.

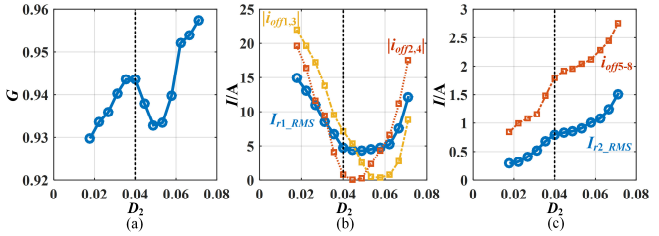
The gain curve with changing D_1 and D_2 under different load conditions are depicted in Fig. 17~19 (a). When the load gets heavier, the voltage gain becomes lower with the same D_1. Under the same load conditions, larger D_1 leads to a greater gain reduction. The variation of output voltage gain is not as ideal as the calculation in Fig. 9 due to the influences of output capacitances of switches, but it has little impact on the changing rule of efficiency.

Moreover, the comparisons of experimentally measured efficiency and calculated efficiency based on loss analysis under the three cases in Fig. 17~19 are shown in Fig. 20. The power conversion efficiency gets higher under heavier load conditions and becomes lower with larger D_1, while the highest efficiency is always reached at D_2=0.5D_1. Under different D_1, D_2 and load conditions, the calculated efficiencies always approach the measured efficiencies, which not only verifies the power loss analysis and efficiency calculation in section III, but also effectively proves the



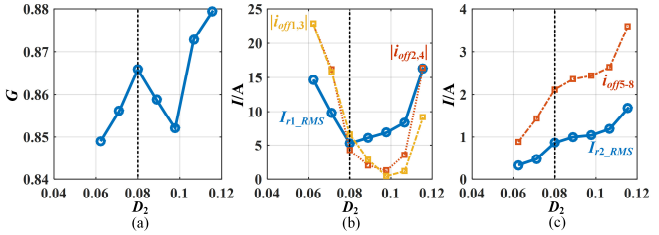
(a) (b) (c)

Fig. 17. Experimental results of EPS control with D_1 = 0.08, D_2 = 0.01~0.08 at 10% load. (a) G. (b) I_{r1_RMS}, $i_{off1,3}$ and $i_{off2,4}$. (c) I_{r2_RMS} and i_{off5-8}.



(a) (b) (c)

Fig. 18. Experimental results of EPS control with D_1 = 0.08, D_2 = 0.01~0.08 at 30% load. (a) G. (b) I_{r1_RMS}, $i_{off1,3}$ and $i_{off2,4}$. (c) I_{r2_RMS} and i_{off5-8}.



(a) (b) (c)

Fig. 19. Experimental results of EPS control with D_1 = 0.16, D_2 = 0.06~0.12 at 10% load. (a) G. (b) I_{r1_RMS}, $i_{off1,3}$ and $i_{off2,4}$. (c) I_{r2_RMS} and i_{off5-8}.

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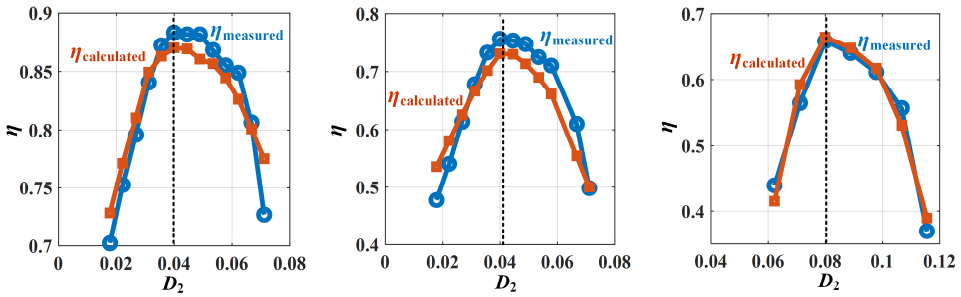

Fig. 20. Experimental and calculated efficiency of EPS control. (a) D_1=0.08, D_2=0.01~0.08, 30% load. (b) D_1=0.08, D_2=0.01~0.08, 10% load. (c) D_1=0.16, D_2=0.06~0.12, 10% load.

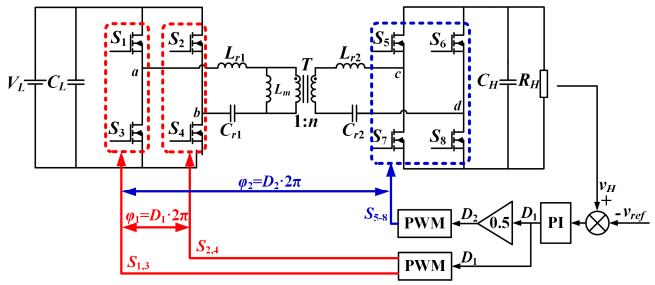

Fig. 21. The block diagram of the EPS control system.

conclusion that the CLLC converter achieves maximum efficiency at D_2=0.5D_1.

B. Closed-loop experiments

Closed-loop experiments are also conducted to compare the performances of EPS control with different combinations of D_1 and D_2, as well as PFM control. The block diagram of the EPS control system is presented in Fig. 21. In EPS control, the switching frequency is kept at resonant frequency. The inner phase-shift ratio D_1 is modulated by the output voltage loop to achieve the reference voltage. The outer phase-shift ratio D_2 is set equal to 0.5D_1 and 0.44D_1 respectively in the two sets of experiments. In PFM control, the switching frequency is directly adjusted by the voltage loop.

Fig. 22 and Fig. 23 present the comparative closed-loop experimental results of D_2=0.44D_1 and D_2=0.5D_1 at 20% and 5% load. The peak-to-peak value and RMS value of resonant current i_{r1} under D_2 = 0.44D_1 are both obviously larger than those of D_2=0.5D_1. Also, ZVS of primary switches is not achieved when D_2 equals 0.44D_1.

Furthermore, Fig. 24 makes a comparison of optimized EPS control and PFM control at 70% load. EPS control always maintains the operation frequency at resonant frequency, while PFM control increases the switching frequency to modulate the output voltage. The steady state operation frequency of PFM is 637.6kHz, which is much higher than the resonant frequency, leading to the loss of soft switching and large switching loss. Therefore, PFM has much lower efficiency than the optimized EPS control with D_2=0.5D_1.

The measured efficiency of EPS control with D_2=0.44D_1 and D_2=0.5D_1 over entire load conditions and PFM control at

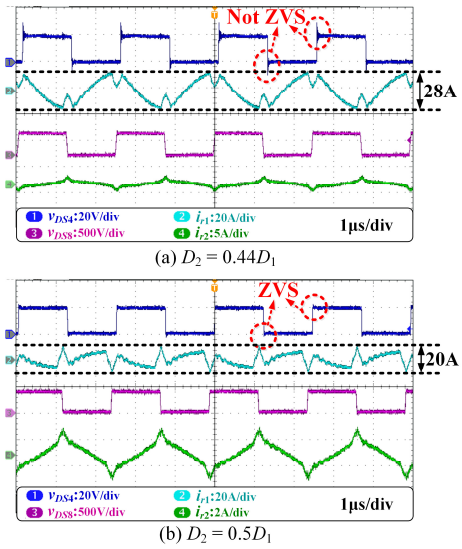

Fig. 22. Comparative closed-loop experiment results of EPS control at 20% load. (a) D_2=0.44D_1. (b). D_2=0.5D_1.

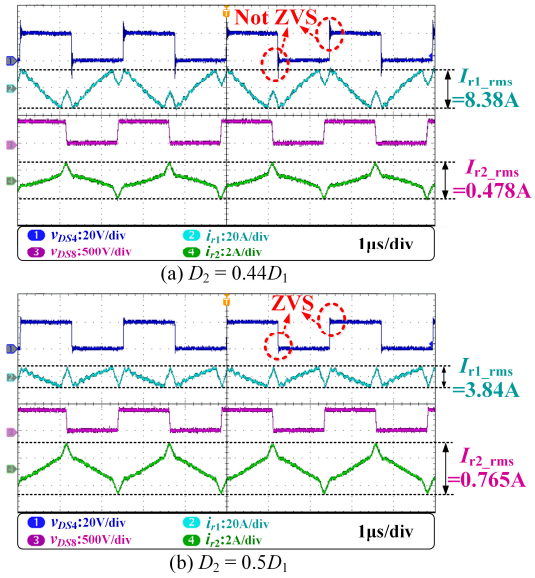

Fig. 23. Comparative closed-loop experiment results of EPS control at 5% load. (a) D_2=0.44D_1. (b). D_2=0.5D_1.

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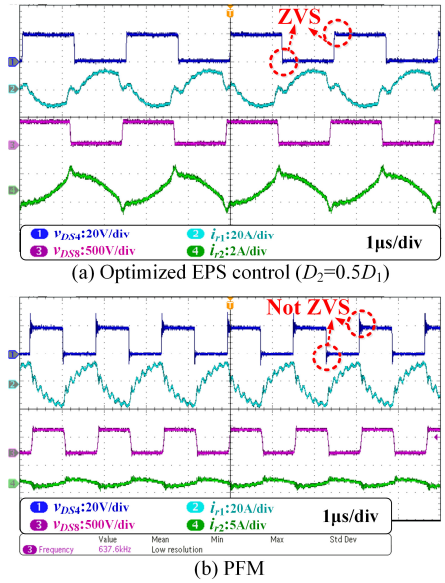

(a) Optimized EPS control (D_2=0.5D_1)

(b) PFM

Fig. 24. Comparative closed-loop experimental results at 70% load. (a) Optimized EPS control with D_2=0.5D_1. (b) PFM control.

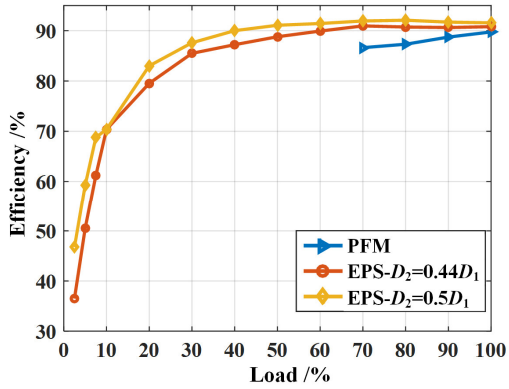

Fig. 25. Measured efficiency of PFM and EPS control with D_2=0.44D_1 and D_2=0.5D_1.

heavy load conditions are shown in Fig. 25. It is demonstrated that the efficiency of optimal EPS control with D_2=0.5D_1 is apparently higher than the efficiency of D_2=0.44D_1, especially at light-loads. Moreover, at heavy load conditions, EPS control also performs better efficiency than PFM control, since the adjusted switching frequency of PFM greatly exceeds the resonant frequency resulting in large switching loss. When the load is below 70%, PFM cannot even regulate the voltage to the reference due to the monotonically increasing gain characteristic in the operation frequency range.

V. Conclusions

To improve the light-load efficiency of full-bridge CLLC resonant converters, this paper proposes an optimization for EPS control to select the optimal and practical combination of inner and outer phase-shifts. First, the voltage gain, RMS values of resonant currents, as well as the time-domain expressions of main circuit variables of EPS control are derived through a detailed circuit modeling and computation. Based on these results, the main power losses including conduction loss, switching loss and core losses of magnetic components are calculated, and the range of ZVS are solved. Through the comprehensive loss analysis, it is concluded that when the outer phase-shift equals the half of the inner phase-shift, the full-bridge CLLC converter achieves maximum efficiency using EPS control. Moreover, for full-bridge CLLC resonant converters with different parameters using different power semiconductors, the operating principle, the analytical modelling and the loss analysis of EPS control are similar, and the conclusion about the optimal ratio between the inner and outer phase-shifts is supposed to be the same. The correctness of the analysis and conclusion is effectively verified by a 21.5V/400V, 200W GaN based CLLC resonant converter prototype. It is demonstrated that the optimized EPS control improves the efficiency over entire load conditions compared with the non- optimized, especially increased by 3.5% under 20% load in comparison with D_2=0.44D_1. Moreover, the efficiency of optimal EPS control also outweighs the efficiency of PFM at heavy-load conditions because of the lower switching frequency and soft switching.

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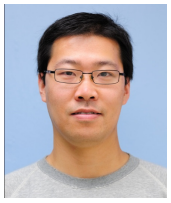

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